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of requests issued from the first bus in the multiple-layer defer queue, wherein each of the requests has corresponding one response selected from the group consisting of a retry response and a defer response to be responded to the first bus;sequentially issuing the requests to the second bus, wherein the requests at least includes a first request;receiving a responded data with respect to the first request from the second bus;providing the responded data to the first bus if the defer response with respect to the first request issues to the first bus; andproviding the responded data to the first bus if the retry response with respect to the first request issues to the first bus and only when the first bus again issues the first request.

- [c8] 8. The method of claim 7, wherein in the step of storing the requests issued from the first bus in the multiple-layer defer queue, the multiple-layer defer queue also provides a request record with respect to each of the requests.
- [c9] 9. The method of claim 8, wherein after the step of providing the responded data to the first bus, the corresponding one of the requests and the request record in the multiple-layer defer queue are deleted.
- [c10] 10. The method of claim 8, wherein the request record comprises:an identification code field, used to store an identification code with respect to each of the requests;a flag field, used to judge whether each of the requests is one selected from the group consisting of the retry response and the defer response; andan effective data field, used to enable the effective data field when the responded data with respect to each of the requests is received.
- [c11] 11. The method of claim 10, wherein when the first bus again issues the first request, an effective bit of the effective data field should be checked to be an enable status, then the responded data is sent to the first bus.
- [c12] 12. The method of claim 7, wherein the requests include one selected from the group consisting of at least one input/output (I/O) read request, at least one I/O write request, and at least one memory read request.
- [c13] 13. A control chip with multi-layer defer queue, coupled to a CPU bus and a PCI bus, the control chip comprising:a PCI request queue, receiving a CPU request

from the CPU bus, and generating a PCI request record; a multi-layer defer queue, when receiving the CPU request, respectively responding to the CPU bus by one of a defer response and a retry response; a PCI access queue, receiving the PCI request record; and a PCI controller, receiving the request from the multi-layer defer queue, causing the PCI request record of the PCI access queue to be transmitted to the PCI bus via the PCI controller; wherein when the PCI bus generates a response data and if the CPU request in the multi-layer defer queue is to produce the defer response, then the response data is directly sent to CPU bus, if the CPU request in the multi-layer defer queue is to produce the retry response and the CPU bus issues the CPU request, then the response data is transmitted to the CPU bus.